

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2000-347929
(43)Date of publication of application : 15.12.2000

(51)Int.Cl. G06F 12/02

(21)Application number : 11-162180 (71)Applicant : NEC ENG LTD
(22)Date of filing : 09.06.1999 (72)Inventor : HONMA MASAKI

(54) MEMORY IC

(57)Abstract:

PROBLEM TO BE SOLVED: To eliminate discontinuous address areas and effectively utilize limited memory resources by remapping calculation to an inputted address on the basis of prescribed information from a non-volatile memory.

SOLUTION: At the time of initial setting, an address bus 10 is connected to a non-volatile memory 12 by a select signal 14. Then, a control signal 15 is made active and a leading address, block size and empty area information are written by using a data bus 17 and a write signal 19. At the time of operation, a signal inputted through the address bus 10 to a memory IC is inputted through a selector 13 to an address translating circuit 11 by the select signal 14. In the address translating circuit 11, the address is remapped on the basis of information for skipping the read of unnecessary addresses from the non-volatile memory 12 and inputted to an internal RAM 16 later. Thus, the read of unnecessary memory spaces is skipped and unnecessary memory spaces can be saved.

